UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/589,403	05/04/2007	Kengo Maeda	559502005300	8227

25227 7590 04/30/2008

MORRISON & FOERSTER LLP
1650 TYSONS BOULEVARD
SUITE 400
MCLEAN, VA 22102

EXAMINER	
ROJAS, DANIEL E	
ART UNIT	PAPER NUMBER
2816	
MAIL DATE	DELIVERY MODE
04/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/589,403	MAEDA ET AL.	
	Examiner	Art Unit	
	DANIEL ROJAS	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-10* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/10/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. Claims 1-3 and 5-6 of this application conflict with claims 1-2 and 4 of Application No. 10/590225. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-3 and 6 are provisionally rejected on the ground of nonstatutory double patenting over claim 1 of copending Application No. 10/590225. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: claim 1 of 10/586403 reads entirely on claim 1 of 10/590225 wherein the active logic value of 10/586403 is a logic "1," claim 2 of 10/586403 reads entirely on claim 2 of 10/590225, claim 3 of 10/586403 reads entirely on claim 2 of 10/590225 and claim 6 of 10/589403 reads entirely on claim 4 of 10590225.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Objections

4. Claim 4 is objected to because of the following informalities: “an extremely short time” is a term of relative degree wherein no value of comparison has been defined (for example, "wherein less than 0.5 seconds or less constitutes an extremely short time”). Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 7 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuzaki et al (US Patent No. 6,088,255), hereinafter referred to as Matsuzaki.

7. For claim 1, Matsuzaki teaches (in his Figure 11) a DLL circuit having a dummy delay (280 and 290, as explained below) corresponding to delay between an internal clock delay (280, which is equal to the delay generated by 800) and an external clock (output of 290 which is equal to the output of 900, as explained below), a variable delay addition circuit (210 and 220) having a means for adjusting delay amount according to a delay amount adjustment signal (output of 400), and a phase comparison circuit (300 and 400) for comparing a phase of an internal clock (output of 800) with a phase of a delay clock input via the variable delay addition circuit (220) and the dummy delay (280 and 290) and outputting the delay amount adjustment signal (output of 400) to the variable delay addition circuit, the DLL circuit comprising: a means for inputting a first signal output during 1 clock cycle of the internal clock to the variable delay addition circuit through the dummy delay at a start of burst (inherent based on the structure of Matsuzaki's Figure 11); and a means for detecting duration time of an active logic value of the first signal input by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay

amount of the variable delay addition circuit based on the duration time at the start of burst (inherent based on the structure of Matsuzaki's Figure 11). Matsuzaki's specification teaches that both the dummy-input buffer 280 and the dummy-data-output buffer 290 have a delay value (column 25, lines 47-49), that the dummy-input buffer 280 has the same delay as the input buffer 800, and that the dummy-data-output buffer 290 has the same delay as the data-output buffer 900 (column 16, lines 1-9).

8. For claim 2, Matsuzaki teaches a DLL circuit having a dummy delay (280 and 290, as explained above) corresponding to delay between an internal clock delay (280, which is equal to the delay generated by 800) and an external clock (output of 290 which is equal to the output of 900, as explained above), a variable delay addition circuit (210 and 220) having a means for adjusting delay amount according to a delay amount adjustment signal (output of 400), and a phase comparison circuit (300 and 400) for comparing a phase of an internal clock (output of 800) with a phase of a delay clock input via the variable delay addition circuit (220) and the dummy delay (280 and 290) and outputting the delay amount adjustment signal (output of 400) to the variable delay addition circuit, the DLL circuit comprising:

a means for inputting a first signal set at a logic "1" during 1 clock cycle of the internal clock to the variable delay addition circuit through the dummy delay at a start of burst (inherent based on the structure of Matsuzaki's Figure 11); and

a means for detecting duration time of the logic "1" of the first signal input by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay amount of the variable delay

addition circuit based on the duration time at the start of burst (inherent based on the structure of Matsuzaki's Figure 11).

9. For claim 3, Matsuzaki teaches a DLL circuit having a dummy delay (280 and 290, as explained above) corresponding to delay between an internal clock delay (280, which is equal to the delay generated by 800) and an external clock (output of 290 which is equal to the output of 900, as explained above), a variable delay addition circuit (210 and 220) having a means for adjusting delay amount according to a delay amount adjustment signal (output of 400), and a phase comparison circuit (300 and 400) for comparing a phase of an internal clock (output of 800) with a phase of a delay clock input via the variable delay addition circuit (220) and the dummy delay (280 and 290) and outputting the delay amount adjustment signal (output of 400) to the variable delay addition circuit, the DLL circuit comprising: a means for inputting a first signal set at a logic "1" during 1 clock cycle of the internal clock to the variable delay addition circuit through the dummy delay as an initialization mode at a start of burst (inherent based on the structure of Matsuzaki's Figure 11); a means for detecting duration time of the logic "1" of the first signal input by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay amount of the variable delay addition circuit based on the duration time as the initialization mode at the start of burst (inherent based on the structure of Matsuzaki's Figure 11); and a clock output means (900) for generating an output clock that synchronizes with the external clock one clock cycle behind with the internal clock delayed by the variable delay addition circuit and with the delay amount corrected by

the phase comparison circuit as a lock mode after the initial setting of the delay amount in the variable delay addition circuit (inherent based on the structure of Matsuzaki's Figure 11).

10. For claim 4, by inspection of Matsuzaki's Figure 11, when the clock signal CLK is not being supplied to 800, the output signal OUT will be stopped (i.e. constant zero value) which can be referred to as a standby mode. When the clock signal CLK is supplied after a standby mode, Matsuzaki's circuit will resume operation. Therefore, the internal clock and the output clock are completely stopped when a reading operation is not performed, thereby achieving a standby mode and a clock can be output in an extremely short time from start of the reading operation.

11. For claim 7, Matsuzaki shows in his Figure 11 that the phase comparison unit receives the output of the variable delay addition circuit as one of its inputs. Therefore, Matsuzaki teaches (inherently) that it is possible to prevent hazard from occurring in a DLL output clock by synchronizing switching timing of delay amount adjustment of the variable delay addition circuit with the output clock of the variable delay addition circuit instead of the internal clock.

12. For claim 10, Makino teaches a phase comparison circuit comprising a multistage inverter (45-47) and a clocked inverter (36, as described below) and comparing a phase of a reference signal (S1) with the phase of a delay signal (S2) at a time when the clocked inverter becomes disabled by a reference clock (as explained below). NAND gate 36 can be considered a clocked inverter since it receives a reference clock signal (S1) and an input delay signal (S2) and is disabled when the

reference clock signal is low. When the reference clock signal is high, the NAND gate works as an inverter which inverts input signal S2. NAND gate 36 is coupled to a first latch comprised of 41 and 42 and a second latch comprised of 43 and 44 which receives the output of 36 through 49. The output of 36 is latched to the first and second latches regardless if the clocked inverter is enabled or disabled. Therefore, a delayed signal is latched when the clock inverter is disabled.

13. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Kikuda et al. (US Patent No. 4,914,326), hereinafter referred to as Kikuda.

14. For claim 8, Kikuda teaches (in Figure 5) a delay circuit comprising an inverter (10) and a transfer gate (20) which is capable of receiving an external voltage to one of the gate inputs of transfer gate wherein variations in the delay time due to variations in power supply voltage can be minimized by supplying electric potential having dependency opposite to increase and decrease in power source voltage to a gate input of the transfer gate.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

17. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki.

18. For claim 6, Matsuzaki shows the details of the variable delay circuits 210 and 220 in Figure 10. As shown, 201 is comprised of four inverters. Examiner takes official notice that it is notoriously old and well known that a common inverter circuit comprises a PMOS transistor with its source connected to a positive power supply and its drain connected to the output, an NMOS transistor wherein the source is connected to ground or a low potential and the drain is connected to the output, and that both said NMOS and PMOS transistors have a gate connected to an input signal. When input signal S1 is low, the first inverter of 201 connects the positive power supply to the output via the PMOS transistor. The output of the first PMOS transistor is inputted to the input of the second inverter, wherein the second inverter connects ground or the low potential power supply to the output. Therefore, the first inverter of 201 (i.e. an inverter circuit) has a positive characteristic in regard to the power supply voltage and the second inverter (i.e. a circuit) has a negative characteristic in regard to the power supply voltage (i.e. the opposite characteristic of the inverter circuit)

19. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable by Makino et al (US Patent No. 4,820,943), hereinafter referred to as Makino.

20. For claim 9, Makino teaches a variable delay addition circuit (Figure 2) having an inverter (20) and a clocked inverter (18) and a register (latch comprised of 19 and 21),

wherein the register automatically stores a logic value of a delay signal (output of 18) at the time when the clocked inverter becomes disabled (Φ bar).

Allowable Subject Matter

21. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

/D. R./
Examiner, Art Unit 2816